Optimization of Nonlinear Figure-of-Merits of Integrated Power MOSFETs in Partial SOI Process

Fan, Lin; Jørgensen, Ivan Harald Holger; Knott, Arnold

Published in:
Proceedings of XXV International Scientific Conference Electronics

Link to article, DOI:
10.1109/ET.2016.7753476

Publication date:
2016

Document Version
Peer reviewed version

Optimization of Nonlinear Figure-of-Merits of Integrated Power MOSFETs in Partial SOI Process

Lin Fan, Ivan Harald Holger Jørgensen and Arnold Knott
Department of Electrical Engineering
Technical University of Denmark
Richard Petersens Plads 325, 2800 Kgs. Lyngby, Denmark
{linfan, ihhj, akn}@elektro.dtu.dk

Abstract – **State-of-the-art power semiconductor industry uses figure-of-merits (FOMs) for technology-to-technology and/or device-to-device comparisons. However, the existing FOMs are fundamentally nonlinear due to the nonlinearities of the parameters such as the gate charge and the output charge versus different operating conditions. A systematic analysis of the optimization of these FOMs has not been previously established. The optimization methods are verified on a 100 V power MOSFET implemented in a 0.18 μm partial SOI process. Its FOMs are lowered by 1.3-18.3 times and improved by 22-95 % with optimized conditions of quasi-zero voltage switching.**

Keywords – **Figure of Merit, Gate Charge, Output Charge, Power MOSFET, Silicon-on-Insulator**

I. Introduction

One of the main challenges for state-of-the art very high frequency (VHF, 30-300 MHz) converters to be effectively used in industrial products is the selection of active components, i.e. power semiconductors [1]. For discrete power devices, the Wide Band Gap (WBG) semiconductors such as GaN and SiC are of consideration [2]. For integration of power devices with control and driver circuits on the same die, one promising way is to use Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs) at different voltage domains in Silicon-on-Insulator (SOI) processes [3].

Conventionally, different transistor technologies are compared quantitatively using figure-of-merits (FOMs) [4]. Another usage of the FOMs is to evaluate the overall performance of a power device for a switching application [5]. The technology or device that has a lower FOM index value is deemed to have a better performance. The early-developed FOM such as Baliga FOM (BFOM) is solely based on the conduction loss minimization [6], and therefore does not apply to high frequency applications where the switching losses are not negligible. As technologies keep developing with emerging devices, different forms of FOMs are proposed in [4], [5], [7], [8]. However, recent researches show that these FOMs are not consistently used [5], [9]. This is because the FOMs typically consist of trade-off parameters such as on-resistance and gate charge (or certain parts of the gate charge), and these contributing parameters depend on the specific operating conditions. As a result, the FOMs are fundamentally nonlinear and application-dependent on voltage and current conditions. A systematic analysis to optimize the nonlinear FOMs has not been previously established, but it is needed to fully explore the performance potentials of the integrated power MOSFETs, especially for partial SOI processes. In Section II, different evaluation methods are reviewed, and the most suitable test circuit for deriving FOMs is selected and implemented. In Section III, the nonlinearities of the gate charge and its different sub-components are analyzed. In Section IV, the FOMs are then synthesized by using the gate charge and other corresponding parameters. Optimization methods of the FOMs versus specific operating conditions are summarized and discussed. Section V concludes the paper.

This research was funded by a grant (No. 67-2014-1) for the TinyPower project from Innovationsfonden, Denmark.

978-1-5090-2883-2 /16/$31.00 ©2016 IEEE

II. Selection and Implementation of Test

Before composing the FOMs of a power MOSFET, the key parameters such as the gate charge and its sub-components have to be known. The first way to obtain various charge parameters is to calculate the integration of the parasitic capacitances as a function of an operating voltage such as the drain-source voltage [4], [10], [11]. However, the calculated results inherently lead to errors. These errors come from the fact that the parasitic capacitances depend on not only the drain-source voltage but also the gate-source voltage [3], which is not taken into account as a variable for the integration calculation. Note that the parasitic capacitances themselves do not provide direct and accurate device-to-device comparisons [12], e.g. a device with a higher capacitance value in [13] switches faster than another device with a lower capacitance value. In addition, a device with a higher on-resistance value in [14] shows a better overall efficiency for a converter, compared to another device with a lower on-resistance value. Therefore, a more accurate way to obtain the gate-charge parameters is needed, particularly for designing a gate-driver circuit [15] as well as calculating the FOMs.

The second way is to simulate the gate-charge behavior during switching transients. There is no standard test circuit for this, and different configurations are compared for choosing the most appropriate test circuit for the purpose of composing the FOMs. Some possible test circuits for evaluating the gate-charge behavior in the transistor turn-on process are shown in Fig. 1. The simplest configuration is to use a resistive load [5], [16], [17], as shown in Fig. 1(a). The configuration that uses a clamped inductive load [18]-[20] is shown in Fig. 1(b). The same circuit in Fig. 1(b) can be reused for a double pulse test (DPT) circuit. By

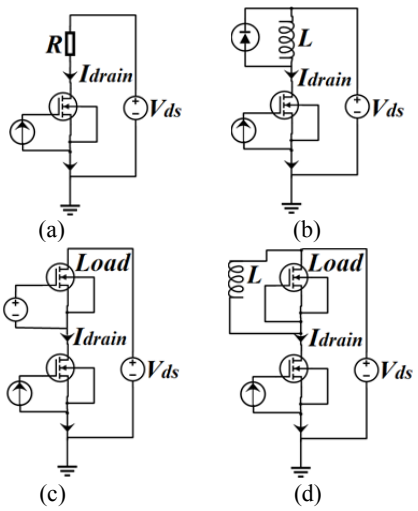

Fig. 1. Several test circuits for gate charge. (a) Resistive load. (b) Clamped inductive load. (c) Active load (simplified bias circuit). (d) Active load combined with an inductive load.

replacing the current source with a voltage-pulse source [21], the transistor turn-on and turn-off energy losses are measured, instead of the gate-charge parameters. For both test circuits in Fig. 1(a) and (b), the voltage transition and current transition occur simultaneously when charging the gate of the transistor. As a result, the sub-components of the gate charge cannot be accurately extracted from the gate-charge curve. Therefore, these test circuits cannot be used for deriving the FOMs that are composed of sub-components of the gate charge.

The configuration that uses an active load [13], [22], [23] is shown in Fig. 1(c) with a simplified bias circuit for the load. Another alternative test circuit is to use a gate-source-shorted active load combined with an inductive load [24], as shown in Fig. 1(d). For both test circuits in Fig. 1(c) and (d), the gate-charge curves are affected by the parasitic capacitances of the active loads as well as the device under test (DUT). Therefore, the resulting gate charge cannot be accounted for solely by the DUT.

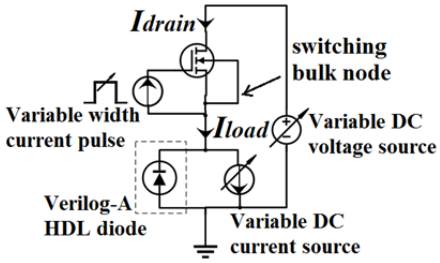

Fig. 2. Selected test circuit for gate charge (for deriving FOMs).

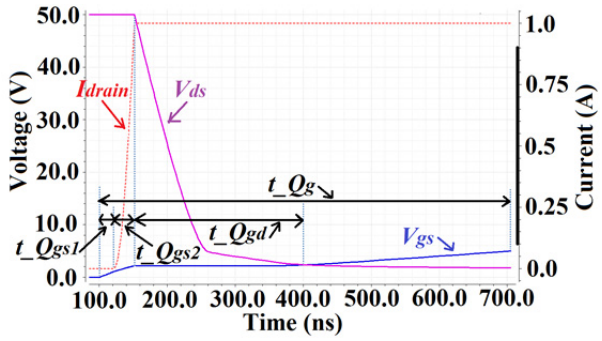

Fig. 3. Simulated transient waveforms and naming conventions.

The principle of the switching power-pole configuration [25] that uses a transistor and a diode is adopted and used for the purpose of deriving different FOMs. With the setup shown in Fig. 2, the voltage and current transitions are separated apart, which results in clear definitions of the sub-components of the gate charge. Provided that the diode is ideal, it is basically equivalent to interchange the positions of the power MOSFET and the load part of the circuit [12], [26]. The bulk terminal of the power MOSFET is connected to the on-chip switching node. This can be done by utilizing the vertical and horizontal dielectric isolation of a partial SOI process. The diode is implemented using the Verilog-A Hardware Description Language (HDL), and it is deliberately modeled with no reverse current and no forward voltage drop. The drain current I_{drain} is always equal to the load current I_{load}.

The DUT is a 100 V power MOSFET implemented in a 0.18 µm partial SOI process with a die area of 0.5276 mm^2. The maximum operating gate-source voltage is 5.5 V. The HiSIM-HV models that are provided by the process foundry are used, which are complete surface-potential-based models based on the drift-diffusion theory [27]. In contrast, the model that is conventionally from a discrete-transistor manufacturer such as [22] uses the most basic Schichman-Hodges model, which is often used for initial manual analysis without considering mobility degradation and an inaccurate model for sub-micron technologies [28]. Using the setup in Fig. 2, the parasitic resistance and/or inductance at the gate terminal do not affect the gate-charge results because the constant-amplitude current pulse is used. The parasitic inductance at the source terminal causes slight errors due to the resulting ringing of the drain current and the drain-source voltage. The results especially for the sub-components of the gate charge are most affected by the parasitic resistance at the source terminal, which is equivalent to adding an extra resistive load to the DUT, as previously discussed for Fig. 1(a).

The simulated transient waveforms are shown in Fig. 3. A current pulse of 1 mA is applied to the gate at 100 ns. The current pulse has a variable pulse width so that the gate-source voltage can be charged to different voltage potentials. The naming conventions are also shown in Fig. 3 and defined as follows: the time interval t_Q_{gs1} starts (t_Q_g starts) when the gate-source voltage V_{gs} starts to increase (i.e. at 100 ns when the current pulse to the gate is applied). The time interval t_Q_{gs2} starts (t_Q_{gs1} ends) when the drain current I_{drain} starts to increase. The time interval t_Q_{gd} starts (t_Q_{gs2} ends) when the drain-source voltage V_{ds} starts to decease. The time interval t_Q_g ends when the final-state (i.e. the state at the end point of the gate-charge event) V_{gs} is reached. The end point of t_Q_{gd} generally has no strict definition, and it is often stated as the point when the final-state V_{ds} or the final-state drain-source resistance R_{ds} (provided that the final-state V_{gs} is high enough to turn the transistor on, the final-state R_{ds} is also called on-resistance) is reached [5], [13], [16], [20], [23], [26]. In fact, both during and after the time interval t_Q_{gd}, V_{gs} still continuously increases (slightly), and the resulting V_{ds} (thus R_{ds}) keeps decreasing, until the final-state V_{gs} is reached. In this paper, the end point of t_Q_{gd} is defined as the intercept point of the extended lines of the V_{gs} curves during and after the time interval t_Q_{gd}.

After the time intervals are obtained, the corresponding charges are calculated as the time intervals multiplied by the gate-charge current. The time interval t_Q_{gs2} multiplied by 1 mA gives so-called Q_{gs2}. The time interval t_Q_{gd} multiplied by 1 mA gives so-called Q_{gd}. The time interval t_Q_g multiplied by 1 mA gives the total gate-charge Q_g.

III. Nonlinearities of Gate Charge

Using the evaluation methods in the previous section, the nonlinearities of the total gate-charge Q_g and its sub-components Q_{gd} and Q_{gs2} versus different operating conditions are shown in Fig. 4. The equivalent R_{ds} is evaluated under the same conditions, and it is derived as the ratio of the final-state V_{ds} to the final-state I_{drain}.

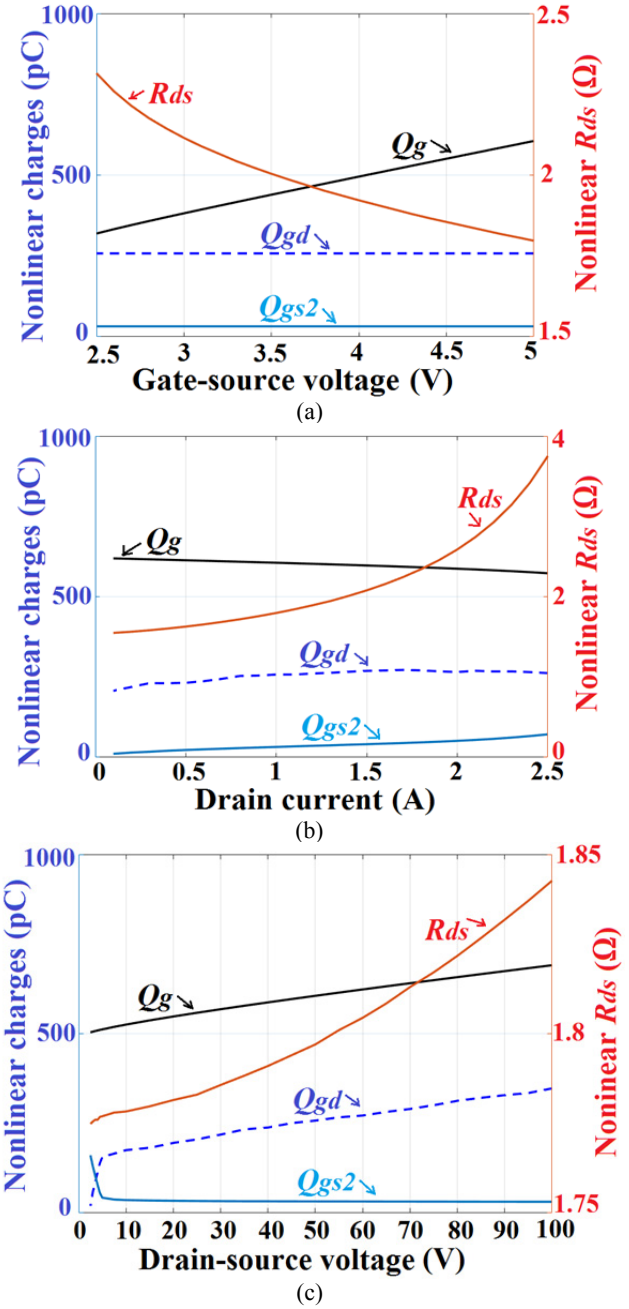

Fig. 4. Gate charge Q_g, its sub-components Q_{gd} and Q_{gs2}, and final-state R_{ds} (simulated). (a) Versus final-state V_{gs} (I_{drain} = 1 A, V_{ds} = 50 V). (b) Versus final-state I_{drain} (V_{gs} = 5 V, V_{ds} = 50 V). (c) Versus original-state V_{ds} (I_{drain} = 1 A, V_{gs} = 5 V).

IV. Optimization of Nonlinear FOMs

The FOMs in (1)-(4) are to be evaluated. FOM_{com1} is commonly used [5], [7]-[9]. FOM_{com2} is also widely accepted [5], [7]. $FOM_{hard\text{-}sw}$ and $FOM_{soft\text{-}sw}$ are proposed in [4] for hard-switching application and soft-switching application, respectively. The soft-switching here generally refers to zero-voltage switching (ZVS) for transistor turn-on transition and/or zero-current switching (ZCS) for transistor turn-off transition.

$$FOM_{com1} = R_{ds} \cdot Q_g \tag{1}$$

$$FOM_{com2} = R_{ds} \cdot Q_{gd} \tag{2}$$

$$FOM_{hard-sw} = R_{ds} \cdot \left(Q_{gd} + Q_{gs2}\right) \tag{3}$$

$$FOM_{soft-sw} = R_{ds} \cdot \left(Q_g + Q_{oss}\right) \tag{4}$$

The output charge Q_{oss} in (4) is analyzed as follows: for

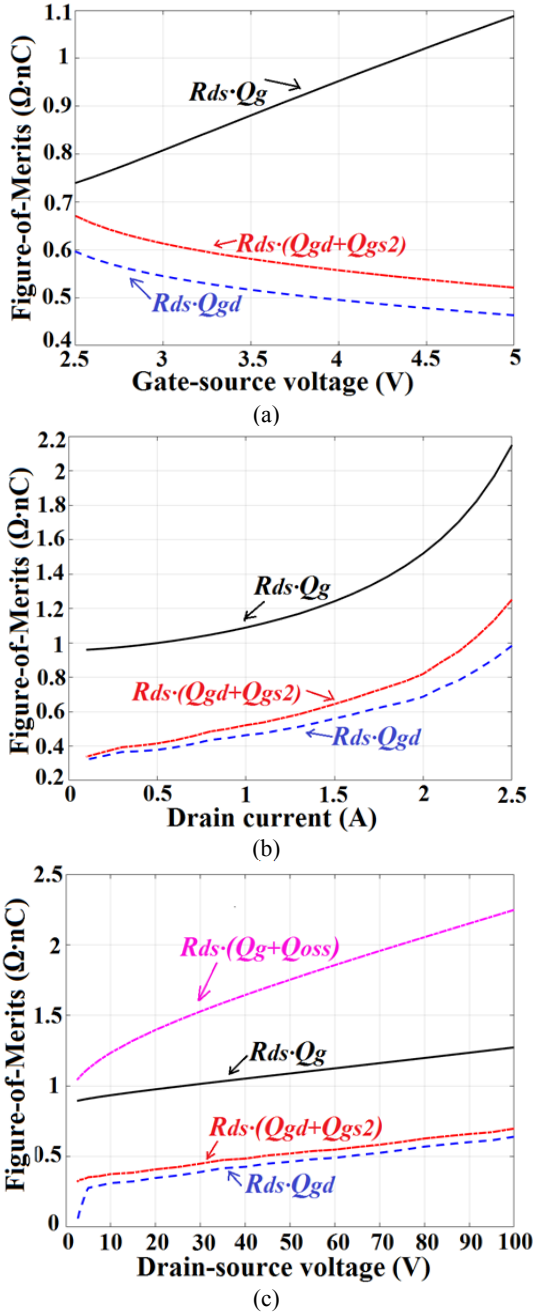

Fig. 5. Nonlinear FOMs (simulated). (a) Versus final-state V_{gs}. (b) Versus final-state I_{drain}. (c) Versus original-state V_{ds}.

TABLE 1. OPTIMIZATION OF NONLINEAR FOMS

Same as in Fig. 5	Best-case FOM vs. Worst-case FOM FOM is lowered: by times (by percentage)			
	FOM_{com1}	FOM_{com2}	$FOM_{hard\text{-}sw}$	$FOM_{soft\text{-}sw}$
V_{gs}	1.5 (32 %)	1.3 (22 %)	1.3 (22 %)	N/A
I_{drain}	2.2 (55 %)	3.0 (67 %)	3.7 (73 %)	N/A
V_{ds}	1.4 (30 %)	18.3 (95 %)	2.2 (54 %)	2.2 (54 %)

the transistor turn-off process, the output capacitance of the power MOSFET is charged to the supply voltage by only a portion of the load current. Therefore, it is difficult to dynamically determine Q_{oss} during the switching transients. Instead, Q_{oss} is estimated with the transistor in the off-state. The gate, source, and bulk terminals are shorted to ground, and the output-charge current is applied to the drain terminal. For the same reason, Q_{oss} (thus $FOM_{soft\text{-}sw}$) is only evaluated versus the drain-source voltage V_{ds}.

The FOMs in (1)-(4) are then derived versus different operating conditions, with the results shown in Fig. 5. The results are also quantitatively summarized in Table 1, versus the same operating conditions as in Fig. 5.

First, the contradicting trends of FOM_{com1} and FOM_{com2} are observed in Fig. 5(a). Another trade-off is between the final-state R_{ds} and the total gate-charge Q_g, as shown in Fig. 4(a). Second, all FOMs in Fig. 5(b) are dominated by R_{ds}. The equivalent R_{ds} increases for high I_{drain} values, due to the quasi-saturation effects and the drain current compression effects [29]. This means that the transistor starts to leave the linear region. Third, Q_{gd} in Fig. 4(c), which dominates FOM_{com2} in Fig. 5(c), quickly vanishes when the original-state (i.e. the state at the start point of the gate-charge event) V_{ds} has a low value (comparable to the V_{gs} values during the time interval t_Q_{gd}). This occurs when the transistor is in the quasi-saturation region before the gate-charge event, with quasi-zero voltage switching. In contrast, if the transistor is forced to be in the linear region, which is closer to the real ZVS, it may not be able to deliver the required final-state I_{drain} or it can deliver the current only after the time interval t_Q_{gd}. Therefore, the operation of the transistor is optimal in the quasi-saturation region rather than deeply in the linear region before the gate-charge event. The maximum improvement of 95 % (theoretically 100 %) is achieved for FOM_{com2}. It indicates that the power MOSFET is suitable for resonant and soft-switching converters (quasi-ZVS is preferred to ZCS).

V. CONCLUSION

A systematic analysis of the optimization of the nonlinear FOMs is performed for a 100 V power MOSFET implemented in a 0.18 µm partial SOI process. The FOMs (compared to the worst-case non-optimized FOMs) are lowered by 1.3-18.3 times and improved by 22-95 % with optimized quasi-zero voltage switching conditions.

REFERENCES

[1] A. Knott, T.M. Andersen, P. Kamby, J.A. Pedersen, M.P. Madsen, M. Kovacevic, M.A.E. Andersen. *Evolution of Very High Frequency Power Supplies*, IEEE Journal of Emerging and Selected Topics in Power Electronics, Vol. 2, No. 3, pp. 386-394, September 2014.

[2] J. Millan. *A Review of WBG Power Semiconductor Devices*, Int. Semiconductor Conference (CAS), pp. 57-66, October 2012.

[3] L. Fan, A. Knott, I.H.H. Jørgensen. *Nonlinear Parasitic Capacitance Modelling of High Voltage Power MOSFETs in Partial SOI Process*, Research Journal Elektronika ir Elektrotechnika, Vol. 22, No. 3, pp. 37-43, June 2016.

[4] A. Lidow, J. Strydom, M.D. Rooij, D. Reusch. *GaN Transistors for Efficient Power Conversion*, 2nd ed., John Wiley & Sons, 2015, pp. 40-54, pp. 90-149.

[5] E. Niculescu, D. Purcaru, M. Maria, M. Niculescu. *A Laboratory Exercise to Estimate the Figure of Merit Index of Power MOSFETs*, Int. Conf. EDUTE, 2009, pp. 56-61.

[6] B.J. Baliga. *Power Semiconductor Device Figure of Merit for High-Frequency Applications*, IEEE Electron Device Letters, Vol. 10, No. 10, pp. 455-457, October 1989.

[7] G. Miller. *Gallium Arsenide (GaAs) Power Stages for Very High Frequency Power Supplies*, PwrSoC, Sarda Technologies, 2012.

[8] F. Hebert, M. Sun, K. Kim, T. Lee, J. Kim, H. Cha, K. Lee, J. Lee, Y. Chen, N. Park, T. Lee. *High-Frequency Power Management Technologies*, PwrSoC, Magnachip, 2014.

[9] J. Ejury. *How to Compare the Figure of Merit (FOM) of MOSFETs*, Infineon Technologies, June 2003.

[10] R.W. Erickson, D. Maksimovic. *Fundamentals of Power Electronics*, 2nd ed., Kluwer Academic, 2001. pp. 92-101.

[11] M.K. Kazimierczuk, D. Czarkowski. *Resonant Power Converters*, 2nd ed., John Wiley & Sons, 2011, pp. 170-175.

[12] V. Barkhordarian. *Power MOSFET Basics*, AN-1084, International Rectifier (Infineon).

[13] *Use Gate Charge to Design the Gate Drive Circuit for Power MOSFETs and IGBTs*, AN-944, International Rectifier (Infineon).

[14] M. Madsen, A. Knott, M.A.E. Andersen. *Low Power Very High Frequency Resonant Converter with High Step Down Ratio*, IEEE AFRICON Conference, pp. 1-6, September 2013.

[15] *Understanding Power MOSFET Data Sheet Parameters*, Rev. 4, AN11158, NXP Semiconductors, February 2014.

[16] *MOSFET Gate-Charge Origin and its Applications*, Rev. 2, AND9083/D, ON Semiconductor, February 2016.

[17] R. Locher. *Introduction to Power MOSFETs and Their Applications*, Rev. B1, Fairchild Semiconductor, October 1998.

[18] *N-Channel PowerTrench MOSFET*, FDP2532/FDB2532, Rev. C2, Fairchild Semiconductor, October 2013.

[19] *Gate Drive Characteristics and Requirements for HEXFET Power MOSFETs*, AN-937, International Rectifier (Infineon).

[20] *Power MOSFET Basics: Understanding the Turn-On Process*, AN850, Vishay Siliconix, June 2015.

[21] A. Anthon, J.C. Hernandez, Z. Zhang, M.A.E. Andersen. *Switching Investigations on a SiC MOSFET in a TO-247 Package*, IEEE IECON conference, pp. 1854-1860, 2014.

[22] *SMPS MOSFET*, IRF5802PbF, International Rectifier (Infineon), April 2010.

[23] *Power MOSFET Basics*, MOS-007, Alpha and Omega Semiconductor.

[24] D. Graovac, M. Purschel, A. Kiep. *MOSFET Power Losses Calculation using the Datasheet Parameters*, v. 1.1, Infineon Technologies, July 2006.

[25] N. Mohan. *Power Electronics, A First Course*, Johm Wiley & Sons, 2012, pp. 24-28.

[26] *MOSFET Basics*, AN-9010, Rev. 1.0.5, Fairchild Semiconductor, April 2013.

[27] *HSPICE Reference Manual: MOSFET Models*, Rev. D-2010.12, Synopsys, 2010, pp. 318-335.

[28] E. Bruun. *CMOS Integrated Circuit Simulation with LTspice IV – a Tutorial Guide,* Bookboon.com, 2015, pp. 67-95.

[29] B.J. Baliga. *Silicon RF Power MOSFETs*, World Scientific Publishing, 2005, pp. 11-49.